IFW 2823

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: David W. Carlson Appln. No.: 09/678,414 Filed: October 2, 2000 For: METHOD FOR PLANARIZING A THIN FILM	Group Art Unit: 2823 Examiner: Kebede, Brook PETITION TO WITHDRAW HOLDING OF ABANDONMENT UNDER 37 CFR 1.181(a)

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a Petition under 37 CFR §1.181(a) requesting withdrawal of a Notice of Abandonment mailed May 28, 2004 in the above-identified application.

1. On November 18, 2003, applicant received an Office Action dated November 14, 2003 in the above-identified application. (Copy attached as Exhibit A.)

2. On January 30, 2004, applicant timely filed an amendment in response to the November 14, 2003 Office Action. (Copy attached as Exhibit B.)

3. The January 30, 2004 amendment included a return receipt postcard. The date stamp on the postcard indicates that the January 30, 2004 amendment was received by the PTO on February 2, 2004. (Copy attached as Exhibit C.)

4. The January 30, 2004 amendment also included a check for $208.00 for 2 extra independent claims and 2 extra total claims. The check was cashed by

the PTO on February 5, 2004 as indicated by the endorsement stamp on the check. (Copy attached as Exhibit D.)

5. On June 1, 2004, applicant received a Notice of Abandonment dated May 28, 2004 in the above-identified application. (Copy attached as Exhibit E).

Thus, since no abandonment of the above-identified application occurred, applicant requests that the Notice of Abandonment be withdrawn and the amendment filed on January 30, 2004 be entered.

Respectfully submitted,

Dated: 6-14-04 By: Mark C. Pickering

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PTO/SB/21 (08-03)
Approved for use through 07/31/06. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/678,414
Filing Date	October 2, 2000
First Named Inventor	David W. Carlson
Group Art Unit	2823
Examiner Name	Kebede, Brook
Total Number of Pages in This Submission: 42	Attorney Docket Number: 100-13602 (P04797-C2)

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Response
  - ☐ After Final (Response)
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Inquiry
- ☒ Other Enclosure(s) *(please identify below)*:
  - **Return Receipt Postcard**
  - **Certificate of Mailing**
  - **Petition to Withdraw Holding of Abandonment Under 37 CFR 1.181(a) with Exhibits A-E**

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Mark C. Pickering, Reg. No. 36,239
Signature	Mark C. Pickering
Date	June 15, 2004

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: M/S Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date: June 15, 2004

Typed or printed name	Robin L. King		
Signature	Robin L. King	Date	June 15, 2004

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,414	10/02/2000	David W. Carlson	~~NSC1-H1700 [P04797]~~ 100-1302	4381

33402 7590 11/14/2003

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/14/2003

2-14-04

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,414	CARLSON, DAVID W.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-7,9,10,13-17,19-25,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 17* is/are allowed.

6)☒ Claim(s) *1,2,5-7,10,13-16,19-25,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 24, 2003 has been entered.

Status of the Claims

2. Claims 1, 2, 5-7, 9, 10, 13-17, 19-25, 27 and 28 are now pending in the application.

Specification

3. The amendment filed on March 25, 2002 in Paper No. 6 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Applicant amend in the specification in Paragraph 5, Page 6 as follows: "As shown in Fig. 3C, **a layer material 342 that lowers resistance** is formed over planarized polysilicon layer 340." Although there is support for formation of "the layer of third material over planarized layer material," there is no support for a layer material 342 (i.e., the layer of third material) that lowers resistance as the specification as originally filed. Applicant is required to cancel the new matter in the reply to this Office Action.

4. The amendment filed on March 3, 2003 in Paper No. 16 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no

amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Claim 22 recites the limitation "forming a layer of third material on the planarized layer of the first material, **the third layer of material lowering the resistance of the first material**" in lines 13-14. However there is no support for the limitation "**the third layer of material lowering the resistance of the first material**" in the specification as originally filed.

Claim 25 recites the limitation "The method of claim 24 and further comprising the step of forming a layer of third material on the planarized layer of material, **the layer of third material and the layer of first material being selectively etched during the selectively etching step**" in lines 1-3.

Claim 25 being dependent of claim 24, the selective etching process provides support for selectively etching for the layer of the first material as the specification as originally filed. However, there is no support for the limitation "the layer of third material being selectively etched during selectively etching process" as recited in claim 25. Therefore, there is no support for the limitation "**the layer of third material being selectively etched during selectively etching process**" in the specification as originally filed.

Claim 26 recites the limitation "The method of claim 25 wherein the layer of third material is conductive" in line 1. Although there is support in the specification for the "third material," there is no support for the third material being "conductive" as the specification originally filed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 19-22, 23, 25 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 22 recites the limitation "forming a layer of third material on the planarized layer of the first material, **the third layer of material lowering the resistance of the first material**" in lines 13-14. However there is no support for the limitation "**the third layer of material lowering the resistance of the first material**" in the specification as originally filed. Therefore, the subject matter is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 25 being dependent of claim 24, the selective etching process provides support for selectively etching for the layer of the first material as the specification as originally filed. However, there is no support for the limitation "the layer of third material being selectively etched during selectively etching process" as recited in claim 25. Therefore, there is no support for the limitation "**the layer of third material being selectively etched during selectively etching process**" in the specification as originally filed. Therefore, the subject matter is not described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 26 recites the limitation "The method of claim 25 wherein the layer of third material is conductive" in line 1. Although there is support in the specification for the "third material," there is no support for the third material being "conductive" as the specification originally filed. Therefore, there is no support for the limitation "**the layer of third material is conductive**" in the specification as originally filed. Therefore, the subject matter is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 19, 20, 21, 23 and 26 are also rejected as being dependent of the rejected independent base claim.

7. Applicant's cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, 5-7, 10, 13-16, 18-25, 27 and 28 rejected under 35 U.S.C. 102(e) as being anticipate by Li et al. (US/6,162,368).

Re claims 1 and 16, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (16); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry until the layer of second material (18) is all removed from the layer of first material (16) to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 2, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 5, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 6, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the first material as being polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 7, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the second material is being an oxide (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 10 as applied to claim 2 above, Li et al. disclose all the claimed limitations including the limitation step of forming a layer of third material on the planarized layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 13, as applied to claim 12 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 14, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation the step of doping the layer of first material prior to forming the layer of second material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 15, as applied to claim 1 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 22, Li et al. disclose a method of planarizing a layer of semiconductor material on a processed wafer (10), the wafer having a top surface (not labeled) , the top surface having a

wafer lower level (not labeled) and a wafer upper level (not labeled) that lies above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface (not labeled), the top surface of the layer of first material (16) having a first lower level (not labeled) and a first upper level (not labeled)that lies above the first lower level; forming a layer of second material (18) on the top surface of the layer of first material (16);chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form planarized layer of first material (see Fig. 2D), the planarized layer of first material (16) covering the wafer upper level (not labeled) of the top surface of the wafer (10); and forming a layer of third material (106 or 114) on the planarized layer of the first material (16) (see Fig. 2D), the third layer of material lowering a resistance of the first layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 19, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the first lower level lies above the wafer upper level (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 20, as applied to claim 19 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 21, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the first material is doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 23, as applied to claim 22 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material makes an electrical contact with a device on the wafer (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 24, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of: forming a layer of first material (16) on the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (60) on the top surface of the layer of first material (16); and chemically-mechanically polishing the layer of second material (18) and the underlying layer of first material (16) with a slurry until the layer of second material (18) is all removed from the layer of first material (16) to form the planarized layer of material; and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level; selectively etching the planarized layer of material that covers (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 25, as applied to claim 24 above, Lin et al. disclose all the claimed limitations including the limitation the step of forming a layer of third material on the planarized layer of

material, the layer of third material and the layer of first material being selectively etched during the selectively etching step (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 27, as applied to claim 24 above, Lin et al. disclose all the claimed limitations including the limitation wherein the layer of first material and the layer of second material are etched with a slurry that etches the layer of first material and the layer of second material at approximately a same rate (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 28, as applied to claim 24 above, Lin et al. disclose all the claimed limitations including the limitation wherein all of the layer of second material is removed during the chemically-mechanically polishing step (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Allowable Subject Matter

10. Claims 9 and 17 are allowed over prior art of record.

Response to Arguments

11. Applicant's arguments filed on August 14, 2003 have been fully considered but they are not persuasive.

With respect to new matter objection under 35 U.S.C. § 132, applicant argued that the specification in page 5, lines 13-16, and page 5, lines 25-27 provides support for the objected recitations. In response to applicant's argument, the Examiner respectfully disagrees with the applicant's contention because none of the added elements as shown in Paragraph 3 and 4 herein above have support in the specification as **the specification originally filed**.

Therefore, the objections under 35 U.S.C. § 132 is deemed proper.

With respect to the claims rejection under 35 U.S.C. § 112 1st Paragraph, applicant argued that the specification in page 5, lines 13-16, and page 5, lines 25-27 provides support for the rejected claims and the amendment do not introduce a new matter. In response to applicant's argument, the Examiner respectfully disagrees with the applicant's contention because none rejected clams as shown in Paragraph 3 and 4 herein above have support in the specification as **the specification originally filed**.

Therefore, the claims rejection under 35 U.S.C. § 112 1st Paragraph is deemed proper.

With respect to claims rejection under 35 U.S.C. §102(e), applicant argued that "step the Li reference teaches two chemical-mechanical polishing steps: a first step that uses slurry 50a to remove native oxide layer 18, and a second step that uses slurry 50b to remove polysilicon layer 16. However, neither of the two chemical-mechanical polishing steps taught by Li can be read to be the chemically-mechanically polishing step required by claim 1..."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits that Li et al. '368 teach all the claimed limitation as shown in Paragraph 9 herein above. In addition, the rejected claim does not call for either single step or prularity step of CMP it just simply recites "chemically-mechanically polishing the layer of second material (330) and the underlying layer of first material (320) with a slurry until the layer of second material (330) is all removed from the layer of first material (320)." And Li et al. teaches that also. Whether one slurry used or multiple slurry utilized is irrelevant the rejected claim is not distinctive form the prior art.

Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Applicant further argued that "Li fails to teach or suggest the formation of a layer of third material, claim 22 is not anticipated by the Li reference. In addition, since claims 19-21 and 23 depend from claim 22, claims 19-21 and 23 are not anticipated by Li for the same reasons as claim 22. With respect to claim 24, this claim recites, in part, selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer." In rejecting claim 24, the Examiner stated, with reference to the selectively etching step, selectively etching the planarized layer of material that covers (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54)." Applicant respectfully has been unable to identify the steps in Li that the Examiner believes reads on the selectively etching step, and has been otherwise been unable to find any discussion in Li that teaches or suggests that polysilicon layer 16 (the layer of first material) is selectively etched when polysilicon layer 16 covers the upper levels of regions 14 as required by claim 24. As a result, claim 24 is not anticipated by Li. In addition, since claims 25 and 27-28 depend either directly or indirectly from claim 24, claims 25 and 27-28 are not anticipated by Li for the same reasons as claim 24."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits that Li et al. '368 disclose formation of the third layer (106) (see

Fig. 2E). Furthermore, with respect to selectively etching step, the argument is moot because applicant fail to provide support for the limitation. However, Lin et al. '368 also disclose the selectively etching step for the third material layer as shown in Figs. 2E and 2F.

Therefore, the rejection under 35 U.S.C. §102(e) is deemed proper.

Conclusion

12. THIS ACTION IS MADE **NON-FINAL**.

Correspondence

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
November 12, 2003

W. DAVID COLEMAN
PRIMARY EXAMINER

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
09/678,414	CARLSON, DAVID W.	
Examiner	Art Unit	Page 1 of 1
Brook Kebede	2823	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	A	US-6,162,368	12-2000	Li et al.	216/89
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	22

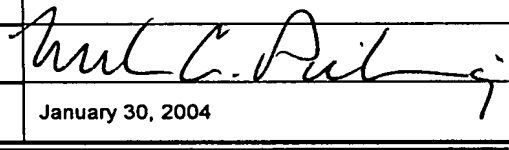
Application Number	10/678,414
Filing Date	October 2, 2000
First Named Inventor	David W. Carlson
Group Art Unit	2823
Examiner Name	Kebede, Brook
Attorney Docket Number	100-13602 (P04797-C2)

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form (in duplicate)
- ☒ Fee Attached (check for $208)
- ☒ Amendment/Response
- ☐ After Final (Response)
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Inquiry
- ☒ Other Enclosure(s) *(please identify below)*:
  Return Receipt Postcard
  Certificate of Mailing
  Definitions from Dictionary.com (3 pages)

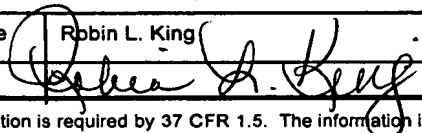
Remarks	**Please charge any necessary fees or credit overpayment to Deposit Account No. 502305. A duplicate copy of this transmittal is attached for this purpose.**

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Mark C. Pickering, Reg. No. 36,239
Signature	
Date	January 30, 2004

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date: January 30, 2004

Typed or printed name	Robin L. King		
Signature		Date	January 30, 2004

FEE TRANSMITTAL

For FY 2004

Patent Fees are subject to annual revision.

Complete if Known	
Application Number	10/678,414
Filing Date	October 2, 2000
First Named Inventor	David W. Carlson
Examiner Name	Kebede, Brook
Group Art Unit	2823
Attorney Document No.	100-13602 (P04797-C2)

TOTAL AMOUNT OF PAYMENT	$208

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge any fees or credit any overpayment under 37 CFR 1.16 and 1.17 which may be required by this paper to Deposit Account No. **502305**
LAW OFFICES OF MARK C. PICKERING

☐ Applicant claims small entity status. See 37 CFR 1.27.

2. ☒ **Payment Enclosed:**
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

LARGE ENTITY Fee Code	LARGE ENTITY Fee ($)	SMALL ENTITY Fee Code	SMALL ENTITY Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility	
1002	340	2002	170	Design	
1003	530	2003	265	Plant	
1004	770	2004	385	Reissue	
1005	160	2005	80	Provisional	
				SUBTOTAL (1)	0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims	Fee from below	Fee Paid
Total Claims	23 - 21 **	= 2	x 18	= $ 36
Independent	7 - 5	= 2	x 86	= $ 172
Multiple Dep.			*	= $ 0

** *or number previously paid, if greater; for Reissues, see below:*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claim in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue ind. claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)	$208

FEE CALCULATION (continued)

3. Additional Fees

Large Entity Fee Code	Large Entity Fee	Small Entity Fee Code	Small Entity Fee	
1051	130	2051	65	Surcharge - late filing fee or oath
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet
1053	130	1053	130	Non-English specification
1812	2520	1812	2520	For filing a request for ex parte reexamination
1804	920	1804	920	Requesting publication of SIR prior to Examiner action
1805	1840	1805	1840	Requesting publication of SIR after Examiner action
1251	110	2251	55	Extension for reply within first month
1252	420	2252	210	Extension for reply within second month
1253	950	2253	475	Extension for reply within third month
1254	1480	2254	740	Extension for reply within fourth month
1255	2010	2255	1005	Extension for reply within fifth month
1401	330	2401	165	Notice of Appeal
1402	330	2402	165	Filing a brief in support of an appeal
1403	290	2403	145	Request for oral hearing
1451	1510	1451	1510	Petition to institute a public use proceeding
1452	110	2452	55	Petition to revive-unavoidable
1453	1330	2453	665	Petition to revive-unintentional
1501	1330	2501	665	Utility issue fee (or reissue)
1502	480	2502	240	Design issue fee
1503	640	2503	320	Plant issue fee
1460	130	1460	130	Petitions to the Commissioner
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)
1806	180	1806	180	Submission of Information Disclosure Stmt
8021	40	8021	40	Recording each patent assignment per property (times number of properties)
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))
1810	770	2810	385	For each additional invention be examined (37 CFR 1.129(b)
1801	770	2801	385	Request for Continued Examination (RCE)
1802	900	1802	900	Request for expedited examination of a design application

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)**	$0

SUBMITTED BY

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Mark C. Pickering, Reg. No. 36,239

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: David W. Carlson Appln. No.: 09/678,414 Filed: October 2, 2000 For: METHOD FOR PLANARIZING A THIN FILM	Group Art Unit: 2823 Examiner: B. Kebede AMENDMENT IN RESPONSE TO OFFICE ACTION MAILED NOVEMBER 14, 2003

INTRODUCTORY COMMENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action mailed November 14, 2003, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper; and

Remarks which begin on page 8 of this paper.

CERTIFICATE OF MAILING

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Dated: January 30, 2004 **By:** Lisa L. Kaag

AMENDMENTS TO THE CLAIMS

1. (Previously Amended) A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.

2. (Original) The method of claim 1 wherein the first lower level lies above the wafer upper level.

3. Cancelled.

4. Cancelled.

5. (Previously Amended) The method of claim 2

wherein the planarized layer of material has a first thickness over the wafer upper level, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to a greater than the first thickness.

6. (Original) The method of claim 1 wherein the first material is polysilicon.

7. (Original) The method of claim 1 wherein the second material is oxide.

8. Cancelled.

9. (Previously Amended) A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the slurry having a selectivity that falls within an approximate range of 0.9-1.1:1.

10. (Original) The method of claim 2 and further comprising the step of forming a layer of third material on the planarized layer of material.

11. Cancelled.

12. Cancelled.

13. (Previously Amended) The method of claim 10

wherein the planarized layer of material has a first thickness over the wafer upper level, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to a greater than the first thickness.

14. (Original) The method of claim 1 and further comprising the step of doping the layer of first material prior to forming the layer of second material.

15. (Original) The method of claim 1 wherein the layer of first material is doped polysilicon.

16. (Previously Amended) The method of claim 1 wherein the layer of first material makes an electrical contact with a device on the wafer.

17. (Previously Amended) A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material, the second layer of material being thicker than the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.

18. Cancelled.

19. (Previously Amended) The method of claim 22 wherein the first lower level lies above the wafer upper level.

20. (Previously Amended) The method of claim 19

wherein the planarized layer of first material has a first thickness over the wafer upper layer, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness.

21. (Previously Amended) The method of claim 22 wherein the first material is doped polysilicon.

22. (Previously Amended) A method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material;

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and

forming a layer of third material on the planarized layer of first material, the third layer of material lowering a resistance of the first layer of material.

23. (Previously Amended) The method of claim 22 wherein the layer of first material makes an electrical contact with a device on the wafer.

24. (Previously Added) A method of forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material;

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of material, the planarized layer of material covering the wafer upper levels and the wafer lower level of the top surface of the wafer; and

selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer.

25. (Previously Added) The method of claim 24 and further comprising the step of forming a layer of third material on the planarized layer of material, the layer of third material and the layer of first material being selectively etched during the selectively etching step.

26. (Cancelled).

27. (Previously Added) The method of claim 24 wherein the layer of first material and the layer of second material are etched with a slurry that etches the layer of first material and the layer of second material at approximately a same rate.

28. (Previously Added) The method of claim 24 wherein all of the layer of second material is removed during the chemically-mechanically polishing step.

29. (New) A method for planarizing a material layer on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

forming a planarized layer of material by chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.

30. (New) A method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material;

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and

forming a layer of third material on the planarized layer of first material, the third layer of material not contacting the wafer lower level and the wafer upper level.

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1-2, 5-7, 9-10, 13-17, 19-25, and 27-30 are now in this application. Claims 3, 4, 8, 11-12, 18, and 26 have been cancelled. Claims 29 and 30 have been added to alternately and additionally claim the present invention. Claims 9 and 17 have been allowed.

The Examiner objected to the amendment mailed on March 15, 2002 under 35 U.S.C. §132 as introducing new matter into the disclosure. In objecting to the amendment, the Examiner indicated that there is support for the formation of a layer of third material over a planarized layer of material, but argued that there is no support for a layer of material 342 that lowers resistance.

The Examiner objected to the amendment mailed on March 4, 2003 under 35 U.S.C. §132 as introducing new matter into the disclosure. In objecting to the amendment, the Examiner argued that there is no support in the specification for the limitations in claim 22 that require that the third layer of material lower the resistance of the first material. In addition, the Examiner argued that there is no support in the specification for the limitations in claim 25 that require that the layer of third material be selectively etched during the selective etching process.

The Examiner rejected claims 19-23 and 25 under 35 U.S.C. §112, first paragraph. In rejecting the claims, the Examiner argued that there is no support in the specification for the limitations in claim 22 that require that the third layer of material lower the resistance of the layer of first material. In addition, the Examiner argued that there is no support in the specification for the limitations in claim 25 that require that the layer of third material be selectively etched during the selective etching process.

In the last amendment, with respect to each of the above rejections which are based on the argument that the specification does not teach a third layer of material that lowers the resistance of the layer of first material, applicant noted that applicant's specification teaches:

> "After this, as shown in FIG. 3B, oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished until oxide layer 330 is substantially, completely

removed from the surface of polysilicon layer 320 to form a planarized layer of polysilicon 340." (See page 5, lines 13-16.)

Thus, applicant's specification teaches that polysilicon layer 320, which can be read to be a layer of first material, and oxide layer 330, which can be read to be a layer of second material, are chemically-mechanically polished to form a planarized layer of polysilicon 340, which can be read to be the planarized layer of material.

In addition, applicant's specification also recites,

> "Once planarized polysilicon layer 340 has been formed, a mask (not shown) is formed and patterned on planarized polysilicon layer 340.
>
> Next, planarized polysilicon layer 340 is etched to form a number of structures, such as local interconnect lines, that are electrically connected to individual devices on wafer 300. (The locations where the structures make electrical contacts with the individual devices of wafer 300 are prepared before polysilicon layer 320 is deposited, and are assumed to be a part of wafer 300.)
>
> Alternately, after the planarization step, one or more additional layers of material, such as materials which lower the resistance of polysilicon, can be formed over layer 340. The mask is then formed and patterned on the additional layers of material which are then etched along with planarized polysilicon layer 340 to form the structures (e.g., local interconnect lines)." [Underlining added.] (See page 5, line 16, to page 6, line 1.)

Thus, if one additional layer of material is used, the one additional layer of material can be read to be a third layer of material, and can be described as a layer of material 342. The Examiner appears to agree with this, stating that there is support for the formation of a layer of third material over a planarized layer of material.

The above section of applicant's specification also indicates that the one additional layer of material can lower the resistance of polysilicon. In responding to applicant's comments, the Examiner stressed that the specification as originally filed does not support the formation of a layer of material over the polysilicon layer that reduces the resistance of the polysilicon layer.

Applicant respectfully does not understand the argument set forth by the Examiner as the originally-filed specification expressly states that one additional layer of material, "such as materials which lower the resistance of polysilicon," can be formed over polysilicon layer

340. Applicant acknowledges that the originally-filed specification does not refer to a layer 342, but this does not prevent the specification from being amended to include a layer 342 when, as in the present case, the specification describes the layer.

Thus, without further direction from the Examiner, applicant does not understand the Examiner's basis for asserting that the originally-filed specification does not support the formation of an additional layer of material, such as a material that lowers the resistance of polysilicon, over planarized polysilicon layer 340, when the originally-filed specification appears to provide all of the necessary support.

Thus, since the originally-filed specification provides the necessary support, the amendment mailed on March 15, 2002 and the amendment mailed on March 4, 2003 do not introduce new matter into the disclosure with respect to the third layer of material lowering the resistance of the layer of first material. For the same reasons, claims 19-23 and 25 satisfy the requirements of the first paragraph of 35 U.S.C. §112 with respect to the third layer of material lowering the resistance of the layer of first material.

With respect to each of the above rejections which are based on the argument that the specification does not teach that the layer of third material is selectively etched during the selective etching process, applicant again respectfully does not understand the arguments set forth by the Examiner. Whenever a mask is formed and patterned, and the exposed regions are then etched, selective etching takes place. Thus, the as-filed specification, as illustrated above, supports selective etching.

As further illustrated above, the as-filed specification teaches, from page 5, line 27 to page 6, line 1, that the

> "mask is then formed and patterned on the additional layers of material which are then etched along with planarized polysilicon layer 340 to form the structures (e.g., local interconnect lines)."

Applicant respectfully does not understand the argument set forth by the Examiner as the originally-filed specification expressly states that one additional layer of material, which can be read to be a layer of third material, is selectively etched (by virtue of the mask) along

with the planarized layer of material, which can be read to be the selective etching process (the etching of the additional layer of material along with polysilicon layer 340).

As a result, without further direction from the Examiner, applicant does not understand the Examiner's basis for asserting that the originally-filed specification does not support a layer of third material that is selectively etched during the selective etching process, when the originally-filed specification appears to provide all of the necessary support.

Thus, since the originally-filed specification provides the necessary support, the amendment mailed on March 4, 2003 does not introduce new matter into the disclosure with respect to the layer of third material and the layer of first material being selectively etched. For the same reasons, claims 19-23 and 25 satisfy the requirements of the first paragraph of 35 U.S.C. §112 with respect to the layer of third material and the layer of first material being selectively etched.

The Examiner rejected claims 1, 2, 5-7, 10, 13-16, 19-25, and 27-28 under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Patent No. 6,162,368). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 1 recites, in part,

> "forming a layer of first material . . .;
> "forming a layer of second material on the top surface of the layer of first material; and
> "chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level."

In rejecting the claims, the Examiner pointed to the step of forming the layer of polysilicon 16 as constituting the step of forming a layer of first material, and the step of forming native oxide layer 18 as constituting the step of forming a layer of second material. The Examiner also argued that the Li reference teaches the chemical-mechanical polishing step required by the claims.

The chemical-mechanical polishing step of claim 1 includes two requirements: (1) the polishing continues "until" the layer of second material is substantially all removed from the

layer of first material, and (2) the polishing forms a planarized layer of material. Applicant respectfully suggests that the Examiner has not given the proper meaning to the word "until" in the present rejection.

A definition of the word "until" is "up to the time of" (we danced until dawn), or "up to the time that" (we walked until it got dark). (See attached definitions from dictionary.com.) Thus, the word "until" defines a point at which an activity stops. The phrase "we danced until dawn" means that the dancers stopped dancing at dawn. Similarly, the phrase "we walked until it got dark" means that the walkers stopped walking when it got dark.

As a result, the phrase "chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material" means that the polishing stops when the layer of second material is substantially all removed from the layer of first material.

In the last amendment, applicant noted that the Li reference teaches two chemical-mechanical polishing steps: a first step that uses slurry 50a to remove native oxide layer 18, and a second step that uses slurry 50b to remove polysilicon layer 16. As shown in FIG. 2C, Li teaches that the first chemical-mechanical polishing step, which uses slurry 50a, stops when all of the native oxide layer 18 (read to be the layer of second material) has been removed from polysilicon layer 16 (read to be the layer of first material).

However, the first polishing step of Li can not be read to be the chemical-mechanical polishing step of claim 1 because the first chemical-mechanical polishing step of Li (slurry 50a) does not "form the planarized layer of material" as required by claim 1. As further shown in FIG. 2C of Li, when all of the native oxide layer 18 (read to be the layer of second material) has been removed from polysilicon layer 16 (read to be the layer of first material) with slurry 50a, the remaining layer of polysilicon 16 still has a severe non-planar topology.

Thus, the first chemical-mechanical polishing step of Li (slurry 50a) does not form a planarized layer of material. Instead, the first chemical-mechanical polishing step of Li exposes the severe topology of polysilicon layer 16. As a result, the first chemical-

mechanical polishing step of Li (slurry 50a) can not be read to be the chemical-mechanical polishing step of claim 1.

In addition, the first and second chemical-mechanical polishing steps can not be read together as a single step because, as a single step, the polishing does not stop until polysilicon layer 16 is planarized as shown in FIG. 2D of Li. Thus, when both polishing steps are read to be a single step, once substantially all of the oxide layer 18 has been removed, the polishing does not stop as required by claim 1, but continues on until polysilicon layer 16 is planarized.

In an attempt to add further clarification, applicant has added new claim 29 which recites, in part,

> "forming a planarized layer of material by chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material, the planarized layer of material lying over the wafer upper levels and the wafer lower level."

Thus, new claim 29 requires that the polishing stop when the layer of second material is substantially all removed from the layer of first material. In Li, the polishing stops when all of the native oxide layer 18 (read to be the layer of second material) has been removed from polysilicon layer 16 (read to be the layer of first material) with slurry 50a. However, as noted above, the remaining layer of polysilicon 16 (read to be the layer of first material) still has a severe non-planar topology which can not be read to be a planarized layer of material.

In responding to applicant's arguments, the Examiner argued that it is irrelevant whether one slurry is used or multiple slurries are used. Applicant notes, however, that the relevance is that when one slurry (50a) is used, the Li reference does not read on the claims. Similarly, when multiple slurries (50a and 50b) are read to be a single etching step, the Li reference still does not read on the claims.

Therefore, since the Li reference does not teach or suggest the chemical-mechanical polishing steps required by claim 1 and new claim 29, claim 1 and new claim 29 are not anticipated by Li. In addition, since claims 2, 5-7, 10, and 13-16 depend either directly or indirectly from claim 1, these claims are not anticipated by Li for the same reasons as claim 1.

With respect to claim 22, this claim recites, in part,

> "forming a layer of third material on the planarized layer of first material, the third layer of material lowering a resistance of the first layer of material."

In rejecting claim 22, the Examiner pointed to the step of forming layer 106 or 114 as constituting the step of forming a layer of third material. However, the structures shown in FIGs. 2E and 2F that are identified by reference numerals 106 and 114 are not a layer of material, but are instead the outer layer of outer polishing pad 100, and a soft layer of polishing pad 110. (See column 3, lines 12-15 and lines 28-29 of Li.) Thus, since Li fails to teach or suggest the formation of a layer of third material, claim 22 is not anticipated by the Li reference. In addition, since claims 19-21 and 23 depend from claim 22, claims 19-21 and 23 are not anticipated by Li for the same reasons as claim 22.

With respect to claim 24, this claim recites, in part,

> "selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer."

In rejecting claim 24, the Examiner asserted that the Li reference teaches "selectively etching the planarized layer of material that covers (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54)." Applicant respectfully has been unable to identify the steps in Li that the Examiner believes reads on the selectively etching step, and has been otherwise been unable to find any discussion in Li that teaches or suggests that polysilicon layer 16 (the layer of first material) is selectively etched when polysilicon layer 16 covers the upper levels of regions 14 as required by claim 24.

In responding to applicant's inability to identify the steps in Li that the Examiner believes reads on the selectively etching step, the Examiner pointed to FIGs. 2E and 2F of Li as teaching a selective etching step. However, from what applicant can determine, the only difference between FIGs. 2E and 2F of Li is that the pads, which do not provide selective etching, have been changed. As a result, claim 24 is not anticipated by Li. In addition, since claims 25 and 27-28 depend either directly or indirectly from claim 24, claims 25 and 27-28 are not anticipated by Li for the same reasons as claim 24.

With respect to new claim 30, this claim recites, in part,

"forming a layer of third material on the planarized layer of first material, the third layer of material not contacting the wafer lower level and the wafer upper level."

Thus, claim 30 requires the formation of a third layer of material, but does not require that the third layer of material lower the resistance of the first layer of material. In addition, new claim 30 is patentable over the Li reference because, as shown in FIG. 2G of Li, if a layer of third material was formed on polysilicon layer 16 (read to be the layer of first material), then the third layer of material must necessarily contact the wafer upper surface (presumably read to be the top surface of oxide region 14).

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

Dated: 1-30-04 By: _____

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3 entries found for *until*.

un·til Pronunciation Key (ŭn-tĭl')
prep.

1. Up to the time of: *We danced until dawn.*
2. Before (a specified time): *She can't leave until Friday.*
3. *Scots.* Unto; to.

conj.

1. Up to the time that: *We walked until it got dark.*
2. Before: *You cannot leave until your work is finished.*
3. To the point or extent that: *I talked until I was hoarse.* See Usage Note at till[2].

[Middle English : un-, *up to* (from Old Norse und. See ant- in Indo-European Roots) + til, *till*; see **till**[2].]

until

\Un*til"\, conj. As far as; to the place or degree that; especially, up to the time that; till. See Till, conj.

In open prospect nothing bounds our eye, Until the earth seems joined unto the sky. --Dryden.

But the rest of the dead lives not again until the thousand years were finished. --Rev. xx. 5.

until

\Un*til"\, prep. [OE. until, ontil; un- (as in unto) + til till; cf. Dan. indtil, Sw. intill. See Unto, and Till, prep.] 1. To; unto; towards; -- used of material objects. -- Chaucer.

Taverners until them told the same. --Piers Plowman.

He roused himself full blithe, and hastened them until. -- Spenser.

2. To; up to; till; before; -- used of time; as, he staid until evening; he will not come back until the end of the month.

He and his sons were priests to the tribe of Dan until the day of the captivity. --Judg. xviii. 30.

Note: In contracts and like documents until is construed as exclusive of the date mentioned unless it was the manifest intent of the parties to include it.

- Roget's Thesaurus - Search for synonyms and antonyms

Patent Appln. No. 09/678,414 File No. 199-13602 By: MCP
In the Matter of the Application of: David W. Carlson
Title: Method for Planarizing a Thin Film
Date Mailed: 01-30-04 Due Date: 02-14-04

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

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- ✓ Other: Definitions from Dictionary.com (3 Pgs.)

1574

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MEMO 100-13602 (2 extra claims/2 extra ind. claims)

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,414	10/02/2000	David W. Carlson	~~NSC1-111700~~ [P04797] 100-13602	4381

33402 7590 05/28/2004

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Abandonment	Application No.	Applicant(s)	
	09/678,414	CARLSON, DAVID W.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *14 November 2003*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☒ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The reason(s) below:

George Fourson
Primary Examiner

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.